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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
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Self calibration of continuous-time filters and systems comprising such filters@

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DESCRIPTION

SELF CALIBRATION OF CONTINUOUS-TIME FILTERS AND SYSTEMS COMPRISING SUCH FILTERS

The present invention concerns the calibration of continuous-time filters, and in particular continuous-time Gm-C and RC-filters.

Continuous-time filters have found increasing commercial applications in telecommunications, video-signal processing, disk drivers, computer communication networks and so forth. A continuous-time filter can be favourably implemented with transconductors and capacitors. Such a filter is called Gm-C filter. If realized using passive resistors and capacitors, the respective filter is called RC-filter.

The frequency characteristics of a filter is determined by the product of the resistance R and the capacitance C in an RC-filter. In a Gm-C filter, the time constant is given by C/G_m.

There is prior art concerning the calibration of the transconductance Gm alone. Such calibrations schemes are not applicable to continuous-time filters, which represent a vast majority of circuits using transconductances. According to the prior art documents listed below, the calibration is achieved by matching the output current of the transconductance - to the input of which a DC signal is applied - to a reference current. A matching error is then used to tune the transconductance:

- US 5,621,355
- US 5,650,950
- US 5,912,583
- US 6,140,867
- US 6,172,569
- EP 561 099

All these prior art documents use the same principle of calibration, while there are certain differences among these documents that only lie in the ways the reference current is being generated. There are also some minor differences in the implementation details. US 5,621,355, for example, requires a precision external resistor, while others documents require a precision current digital-analog converter (DAC). According to US 5,621,355 the reference current is generated by applying an accurate DC voltage, while in US 5,650,950, US 5,912,583, US 6,140,867, and US 6,172,569 the desired transconductance Gm is mapped to a reference current by a digital signal applied to the DAC. EP 561 099 proposes to use a polarization circuit to do the calibration.

There are application limitations for these prior art schemes. The requirement of an external precision resistor, a precision DAC, and a precision DC voltage make these schemes expensive. Another disadvantage is that the calibration is done at DC.

The scheme presented in US 5,621,355 is actually a modification of a previous publication by Laber and Gray in IEEE Journal of Solid-State Circuits, Vol. 28, No. 4, April 1993, where only Gm is tuned. The modification was to replace the external resistor by a switched-capacitor acting as a resistor. As above, the calibration is to match the transconductance Gm to that of an external precision resistor by forcing the same voltage over both the resistor and the input of the transconductor Gm.

Yet another approach is disclosed in US 6,304,135. According to US 6,304,135, Gm is determined by an external resistor R_{ext} and C is calibrated iteratively by compensating an on-chip calibrating capacitor with a very complex variable current source. A special algorithm is required to perform the iterative calibration. The variable current source proposed in US 6,304,135 is complex. The calibration approach only works with the one transconductor type described in US 6,304,135 and the approach is not applicable to other types of transconductors.

The calibration scheme presented in US 6,084,465 works in a different manner. After a discharge is completed, one capacitor is charged by the master Gm within a certain time interval, the capacitor voltage at the end of this time interval then being compared with a fixed voltage. An error signal is then used to tune the Gm. In order to preserve this voltage while the capacitor is in discharge, another capacitor with switches is required. Both capacitors have to be perfectly matched which is not possible in practice thus resulting in errors. It is another disadvantage of this scheme, that a very complex state machine is required to control various switches. Furthermore, the whole calibration takes quite long.

A variation of the scheme presented in US 6,084,465 is described in US 6,111,467. This scheme is complex too, and it requires many switches and switching activities.

A very complicated and complex scheme is described in US 6,112,125. The tuning is achieved by injecting a reference signal and monitoring the phase of a filter output.

The big advantage of a Gm-C filter over an RC-filter is the tuning ability of the filter via the transconductance G_m. However, both filter types suffer from process variations, thus limiting them only to non-critical applications.

Self calibration is an effective technique to surmount the problem and to realize more accurate continuous-time filters. Almost all known calibration techniques are based on the so-called master-slave principle. Both the slave filter, which processes the signal, and the master control block, which may be either comprise a voltage-controlled oscillator (VCO) or a voltage controlled filter (VCF), are made of identical transconductors controlled by a voltage. After the master control block, which is put within a phase-locked loop (PLL), is calibrated or tuned to a reference frequency of the PLL, its time constant (τ) is tuned to the correct value. If the transconductors and capacitors in both master and slave are perfectly matched, the slave filter is also tuned to its desired characteristics. It is a disadvantage of conventional calibration techniques

that a VCO or VCF requires at least two integrators, i.e., at least two transconductors and some capacitors. The tuning precision is relative poor because of the internal mismatches. In addition, the power consumption and the required area are considerably large.

A basic lossless Gm-C integrator 10 is illustrated in Fig. 1. The Gm-C integrator 10 comprises a transconductor 13 having a voltage input 12. Another input 15 is connected to ground. A capacitor C is arranged between the transconductor output 14 and ground. The integrator's transfer function is given by

$$\frac{V_0}{V_{in}} = \frac{1}{s\tau} \qquad (1)$$

where τ is the time constant of the integrator 10, determined by the capacitor C and the transconductance G_m of the transconductor 13:

$$\tau = \frac{C}{G_m} \qquad (2)$$

In an RC filter, the time constant τ is the product of R and C. In an integrated Filter, both G_m or C are subject to process variations and so are the characteristics of the whole filter, too. It is an advantage of Gm-C filter, that G_m is controllable. G_m can be controlled by varying the voltage υ (herein also referred to as control signal) that is applied to an input 11 of the transconductor 13. By an appropriate arrangement Gm-C filters can be made to be self calibrated.

Currently, continuous-time Gm-C filters or RC filters are confined only to non-critical applications due to process variations, if no special measures are taken.

It is another object of the present invention to provide filter systems that avoid or reduce disadvantages of known filter systems.

It is an object of the present invention to provide a scheme for flexible calibration of continuous-time Gm-C filters and RC-filters.

SUMMARY

These and other objectives are achieved by the present invention which provides filter systems according to claim 1 and implementations, according to claim 15, using such filter systems.

Advantageous implementations are claimed in the dependent claims 2 through 14.

This proposal discloses a technique that overcomes all of the above mentioned problems by using just one transconductor or resistor and one capacitor in the master control unit. Other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

Brief description of the drawings

For a more complete description of the present invention and for further objects and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a schematic block diagram of a conventional lossless Gm-C integrator,

FIG. 2A is a schematic block diagram of a master control block, according to the present invention,

FIG. 2B is a graph giving the definition of ξ,

FIG. 3 is a schematic block diagram of a filter system, according to the present invention,

FIG. 4A is a schematic block diagram of a logic circuit, according to the present invention,

FIG. 4B is a graph showing various signals, according to the present invention,

FIG. 5 is a schematic block diagram of a phase frequency comparator (PFC), according to the present invention,

FIG. 6 is a graph showing other signals, according to the present invention,

FIG. 7 is a schematic block diagram of a VCC that can be used in an RC filter, according to the present invention.

Fig. 2A illustrates the principle of the proposed self calibration scheme. It is based on the master-slave principle. However, the master is neither a VCO nor a VCF, as in prior art systems. Instead, it comprises an integrator 20 similar to the integrator 10 shown in Fig. 1. According to the invention, a DC voltage V_B is applied to the input 22 of a transconductor 23, which is followed by a comparator 25. A capacitor C is arranged between the transconductor output 24 and ground. The voltage V_C over the capacitor C can be expressed as

$$V_C = \int \frac{G_m V_B}{C} dt = \frac{V_B t}{\tau} \qquad (3)$$

Referring to the graph in Fig. 2B, if the initial value of the voltage V_C at the transconductor output 24 is zero, the time t that it takes for V_C to reach the threshold level V_{th} of the comparator 25 is given by

$$\xi = \tau V_{th} / V_B \tag{4}$$

Rewriting the above equation yields the time constant of interest

$$\tau = \xi V_B / V_{th} \tag{5}$$

Therefore, the time constant τ of a salve filter, defined in eq. (2), can be calibrated or tuned either by varying V_{th}, or V_B, or ξ, or any combination of theses parameters. Defined in Fig. 2B, the parameter ξ is a time quantity and can be made very accurate in a way as presented below.

Based on the principle shown in Figs. 2A and 2B, the block diagram of the proposed self calibration scheme for Gm-C filters is presented in Fig. 3, where the capacitors in the slave filters 27.1 – 27.5 are not shown. In addition to the integrator 30, the capacitor C, the transconductor 33, and the comparator 35, the master control block 36 comprises a phase-frequency comparator (PFC) 28, and a switch 39, controlled by the signal V_S. The switch 39 is arranged in parallel to the capacitor C. The transconductors 33 both in the master control block 36 and the slave filters 27.1 – 27.5 are controlled by the control signal υ of the phase-frequency comparator 28. Both signals V_S and the reference frequency f_{ref} are derived from a clock signal CK, as schematically indicated in Fig. 3. A logic circuit 40 is employed to provide the signals V_S and f_{ref}. Details of an exemplary logic circuit 40 are given in Fig. 4A. The logic circuit 40 receives a clock signal CK as input signal. Such a clock signal is generally available on chip.

The operation of the logic circuit 40 – as illustrated in Fig. 4A - is as follows: The input clock CK is first delayed by two delay elements 51 and 42, thus generating two delayed versions of the clock signal CK, designated as dl1, which is inverted, and dl2. The frequency of the input clock, f_{CK}, is divided by two by the flip-flop (FF1) 43, which is assumed to be a positive edge-triggered flip-flop. This is why its clock signal is first inverted by means of an inverter 44. The signal dl2 is applied as clock signal to a second preset flip-flop (FF2) 45. A set signal (set) is generated by a logic combination of CK, dl1 and qn2. In the present example, the logic combination is performed by the two gates 46 and 47. The Q-output 48 of the flip-flop (FF2) 45 goes logic high whenever the set signal (set) is logic low. Two gates 49 and 50 are employed at the output side of the logic circuit 40 in order to provide the output signal V_S that is employed to control the switch 39. The interdependence of the signals is illustrated in the graphs of Fig. 4B.

Now back to Fig. 3. When the output signal V_S is logic high, the switch 39 is closed and the capacitor C discharges. During this time, the reference frequency signal f_{ref} is logic low (see the diagrams in Figs. 4B and 6). As soon as f_{ref} switches to logic high, V_S goes back to logic low. The switch 39 is opened again and the transconductor 33 starts to charge the capacitor C. As long as V_C is below the threshold voltage V_{th} of the comparator 35 (cf. Fig. 6), the output signal f_{com} at the output 29 of the comparator 35 remains logic high. The output signal f_{com} switches to logic low as soon as V_C exceeds the threshold voltage V_{th} of the comparator 35. The PFC 28 (e.g., comprising a PFD and a loop filter) generates the control signal υ and applies it to the input 31 in such a way that the phase difference between f_{ref} and f_{com} becomes zero. In other words, the PFC 28 compares the phases and the frequencies of the input signals f_{ref} and f_{com}. One has

$$\xi = T \qquad (6)$$

where T is the period of the input clock CK (cf. Fig. 4B). Substituting eq. (6) into eq. (5) yields

$$\tau = TV_B / V_{th} \qquad (7)$$

In other words, according to the present invention a filter system with self-calibration means is provided, as illustrated in Fig. 3. The system comprises a master control unit 36 and a slave unit with one or more slave filters 27.1 – 27.n. The master control unit 36 as such comprises an integrator 30 having circuit elements which match those circuit elements of the slave filter 27.1 – 27.n that define the slave filter's time constant τ. According to the present invention good matching is achieved, if the ratio of Gm of the master to Gm of a slave filter is constant. The same should apply to the ratio of the capacitance of the master to the capacitance of the slave filter. Furthermore, the master control unit 36 comprises a voltage comparator 35 being connected to an output 34 of the integrator 30. The voltage comparator 35 is employed to provide an output frequency signal f_{com} at the output 29. There is a so-called phase frequency comparator (PFC) 28 that provides a control signal υ as output signal. The phase frequency comparator 28 receives the output frequency signal f_{com} and a reference frequency signal f_{ref} as input signals. The slave unit comprises at least one slave filter 27.1 – 27.n. Each slave filter has a control signal input 41 for receiving the control signal υ that allows to calibrate the slave filter's transfer function by influencing the slave filter's time constant τ. In Fig. 3, an embodiment is shown where the transfer functions of all five slave filters 27.1 – 27.n are calibrated by a common control signal υ.

According to the invention, the time constant τ is calibrated by tuning G_m. This is done by periodically charging the capacitor C of the master control block 36 within a certain time interval of the clock signal CK. The comparator 35 is employed to compare the voltage V_C over this capacitor C with a predefined voltage V_{th}, thus generating a periodic signal f_{com}. By using a PLL, the time constant τ to be tuned can be made to be equal to the period T of the clock signal CK. This is very convenient in practice. The time constant τ of a large range can be calibrated by adjusting the clock frequency f_{CK}.

Details of a phase frequency comparator 28 are illustrated in Fig. 5. The PFC 28 may comprise a loop filter 52 having an output 31 and providing the control signal υ as output signal at this output 31. The phase frequency comparator 28 may further comprise a phase frequency detector (PFD) 53 arranged in front of the loop filter 52. The phase frequency detector 53 has two inputs. It receives the output frequency signal f_{com} and a reference frequency signal f_{ref} as input signals. In the present embodiment, the PFD 53 is designed to operate on the falling edges 54 and 55 of the output frequency signal f_{com} and the reference frequency signal f_{ref}, as indicated in the graph of Fig. 6. An error signal x representing the phase difference between the output frequency signal f_{com} and the reference frequency signal f_{ref} is being fed by the phase frequency detector 53 to the loop filter 52 in order to enable the loop filter 52 to provide the control signal υ as output signal. The graph of Fig. 6 gives further details about the timing and the self calibration according to the present invention.

According to known calibration techniques, a VCO or VCF in the master control unit is tuned to the reference frequency of a PFD. By contrast, the time constant τ presented in connection with the present invention depends on three circuit parameters: the input DC voltage V_B at the input 32, the threshold voltage V_{th} of the comparator 35, and the period T of the input clock signal CK, as expressed by eq. (7). According to the present invention, there is, therefore, a high degree of freedom and flexibility in calibrating Gm-C filters: Varying one, two, or even all three circuit parameters V_B, V_{th}, T simultaneously. This is one of the most salient features the inventive calibration scheme possesses. Consider the case of varying just one circuit parameter:

1) Tuning the G_m by the input clock frequency f_{CK} while keeping V_{th} and V_B unchanged. For this calibration strategy, the time constant τ is tuned by varying the clock frequency f_{CK}, which is the reciprocal of the input clock period T. As a result, the time constant τ is tuned to the product of the input clock period T and the V_{th} to V_B ratio, as given in eq. (7). Particularly, if $V_{th} = V_B$, one obtains

$$\tau = T \qquad (8)$$

Similarly, if $V_{th} = 2V_B$, one has $\tau = T/2$ and if $V_{th} = V_B/2$, $\tau = 2T$, etc.

From eq. (8) it is apparent that this calibration strategy offers the highest calibration accuracy, which is the same as that of the input clock, and this accuracy maintains over the entire tuning range. Also $\tau = T$ makes it very attractive in practice.

2) The time constant τ can be made proportional to V_B if V_{th} and f_{ref} are keept unchanged. In this case, the available tuning range may be limited by the input range of the transconductor 33.

3) The time constant τ can be made inversely proportional to V_{th} if V_B and f_{ref} are left unchanged. This calibration strategy makes it possible to tune the time constant τ over a larger range by a smaller variation in V_{th}. To demonstrate this, a numeric example is considered. Assuming the default value for V_B is 1V and the corresponding transconductance is G_{m0}, the following table is obtained:

Calibration strategy 2)	Tuning voltage V_B [V]	1	2	4	8
Calibration strategy 3)	Tuning voltage V_{th} [V]	1	0.5	0.25	.125
G_{m0}		G_{m0}	$2G_{m0}$	$4G_{m0}$	$8G_{m0}$

It is seen that in order to tune G_m by a factor of 8, this calibration strategy requires V_{th} to change only from 1 to 0.125 = 0.725V. By contrast, the calibration strategy 2) entails a varying range of as large as 7V.

According to the present invention, it is also possible to allow two or even all three circuit parameters to vary simultaneously to calibrate the Gm-C filter. This is particularly useful in applications where a wider tuning range is required.

In the following, the calibration of RC filters is addressed. So far the present specification was mainly targeted at Gm-C filters. The proposed calibration technique can be directly applied to RC filters, too. The only change is that one has to replace the transconductor in the master control block by a voltage-to-current converter (VCC). The ~~purpose is to have a transconductance derived from a resistor of the same type as used~~ in the slave RC filters.

One possible embodiment of such a converter is depicted in Fig. 7. An operational amplifier 61 (op-amp) drives two matched pMOS transistors 62 and 63. Assuming an infinite amplifier gain, a feedback via a connection 64 will force the voltage V_1 over a resistor R to be equal to V_B, resulting in a transconductor of the value:

$$G_m = 1/R \tag{9}$$

Note that according to the present invention this VCC 60 is only needed in the master control block. Fig. 7 assumes that the resistors R in both the master control block and the slave filters are controlled by the voltage υ. In fact, the proposed calibration technique allows to vary either R or C. This is accomplished by replacing resistors or capacitors by so-called programmable resistor arrays (PRA) or programmable capacitor arrays. A programmable resistor array is an array or tree of resistors with a number of switches and a programmable capacitor array is an array or tree of capacitors with a number of switches.

While the time constant τ can be tuned/calibrated continuously with Gm-C filters, the calibration of a RC filter is in steps. In binary programmable element arrays, the steps are determined by the smallest segment in the array.

The present invention is well suited for being used in a baseband integrated circuit (IC) designed for GSM transceivers, for example. In such a GSM transceiver, in the transmitter path a 3rd order Butterworth lowpass (LPF) filter is required to suppress the

image components of the GMSK modulated signal after a transmitter digital-to-analog converter (DAC) at 4.33MHz. Being an RC-type filter and no calibration or tuning being provided, the filter would be very vulnerable to process variations. As the resistance used can vary as large as -13% and +33%, and the capacitance +/-10%, it is quite difficult to achieve both sufficient image rejection and maximum flatness up to 100kHz in the passband when using conventional approaches. If the time constant τ was too large, the 3dB frequency would be shifted to a lower frequency, whereas this does not cause concern in the image rejection, it does for the baseband signal. Similarly, there might be concerns with the image rejection if the time constant τ was too small due to process variations. Furthermore, if the process had shifted, or if a new application or system was foreseen, a complete redesign would be inevitable.

Such a redesign can be avoided if the self calibration according to the present invention is employed. Adding self calibration capability to continuous-time filters targeted at critical applications can greatly reduce the time-to-market cycle, greatly reduce the costs, and greatly enhance the system performances.

As an example to verify the calibration scheme according to the present invention, a 3rd-order Gm-C filter has been designed, using the proposed calibration strategy 1). Simulation results indicate that the calibration process, without any optimization, takes only less than 9 cycles of the reference frequency f_{ref} to complete. The time constants τ, both in the master control block and the slave filters, become error-free after the calibration.

Filter systems according to the present invention are based on a self calibration technique using only one transconductor and one capacitor. The master control block is not a VCO or VCF.

The invention is very well suited for accurate, integrated continuous-time filters, such as continuous-time Gm-C filters (using transconductors and capacitors) or continuous-time RC filters (using passive resistor and capacitors).

The invention offers a high degree of freedom and flexibility in choosing a calibration strategy. The circuits proposed are robust and the calibration is efficient and can be done with high precision. It is a further advantage that no external elements are required. The inventive scheme is very attractive for low-cost integration. There are no application limitations at all.

Filter system according to the present invention are based on the so called master-slave principle.

It is appreciated that various features of the invention which are, for clarity, described in the context of separate embodiments may also be provided in combination in a single embodiment. Conversely, various features of the invention which are, for brevity, described in the context of a single embodiment may also be provided separately or in any suitable subcombination.

In the drawings and specification there has been set forth preferred embodiments of the invention and, although specific terms are used, the description thus given uses terminology in a generic and descriptive sense only and not for purposes of limitation.

CLAIMS

1. Continuous-time filter system with self-calibration means, the system comprising a master control unit (36) and a slave unit with at least one slave filter (27.1 – 27.n),

- the master control unit (36) comprising
  - an integrator (30) having circuit elements (33, C) which match those elements of the slave filter (27.1 – 27.n) that define the slave filter's time constant (τ),
  - a voltage comparator (35) connected to an output (34) of the integrator (30), the voltage comparator (35) providing an output frequency signal (f_{com}), and
  - a phase frequency comparator (PFC; 28) providing a control signal (υ) as output signal, the phase frequency comparator (PFC; 28) receiving said output frequency signal (f_{com}) and a reference frequency signal (f_{ref}) as input signals,
- the slave unit comprising said at least one slave filter (27.1 – 27.n), the slave filter (27.1 – 27.n) having a control signal input (41) for receiving said control signal (υ) thus allowing to calibrate the slave filter's transfer function by influencing the slave filter's time constant (τ).

2. The system of claim 1, wherein the slave filter is an RC-filter and the control signal (υ) is a discrete signal leading to a calibration of the slave filter's transfer function in steps.

3. The system of claim 1, wherein the slave filter is a continuous-time Gm-C-filter and the control signal (υ) is a continuous signal.

4. The system of claim 1, 2 or 3, wherein the slave filter is an integrated filter.

5. The system of one of the preceding claims, wherein the master control block (36) comprises one transconductor (33) and one capacitor (C) only.

6. The system of one of the preceding claims, wherein the phase frequency comparator (PFC; 28) comprises:

- a loop filter (52) providing the control signal (υ) as output signal,
- a phase frequency detector (PFD; 53) situated in front of the loop filter (52), the phase frequency detector (PFD; 53) receiving said output frequency signal (f_{com}) and a reference frequency signal (f_{ref}) as input signals,
- an error signal (x) representing the phase difference between the output frequency signal (f_{com}) and the reference frequency signal (f_{ref}) being fed by the phase frequency detector (PFD; 53) to the loop filter (52).

7. The system of one of the preceding claims, wherein the master control unit (36) comprises a switch (39) being controllable by a signal (V_S).

8. The system of claim 7, wherein a logic curcuit (40) is employed in order to provide the signal (V_S) and the reference frequency signal (f_{ref}), both signals (V_S) and (f_{ref}) being derived from a clock signal (CK).

9. The system of one of the preceding claims, wherein a DC voltage (V_B) is applied to an input (32) of the integrator (30).

10. The system of one of the preceding claims, wherein the integrator (30) has a transconductance (Gm) that can be tuned by varying

- a threshold voltage (V_{th}) being applied to an input of the voltage comparator (35), and/or
- a DC voltage (V_B) being applied to an input (32) of the integrator (30), and/or
- the frequency (f_{CK}) of a clock signal (CK).

11. The system of one of the claims 1 through 9, wherein the integrator (30) has a transconductance (Gm) that can be tuned by varying an input clock frequency (f_{CK}) of a clock signal (CK) while keeping a threshold voltage (V_{th}) being applied to an input of the voltage comparator (35) and a DC voltage (V_B) being applied to an input (32) of the integrator (30) unchanged.

12. The system of one of the claims 1 through 9, wherein the integrator (30) has a transconductance (Gm) that can be tuned by varying a DC voltage (V_B) being applied to an input (32) of the integrator (30) while keeping a threshold voltage (V_{th}) being applied to an input of the voltage comparator (35) and the reference frequency signal (f_{ref}) unchanged.

13. The system of one of the claims 1 through 9, wherein the integrator (30) has a transconductance (Gm) that can be tuned by varying a threshold voltage (V_{th}) being applied to an input of the voltage comparator (35) while keeping a DC voltage (V_B) being applied to an input (32) of the integrator (30) and the reference frequency signal (f_{ref}) unchanged.

14. The system of claim 1, wherein the master control block (36) comprises a voltage-to-current converter (VCC; 60) and/or a programmable resistor array (PRA) and/or a programmable capacitor array.

15. Telecommunication system, video-signal processing system, or disk driver system comprising a system in accordance with at least one of the claims 1 through 14.

ABSTRACT

SELF CALIBRATION OF CONTINUOUS-TIME FILTERS AND SYSTEMS COMPRISING SUCH FILTERS

Continuous-time filter system with self-calibration means. The system comprises a master control unit (36) and a slave unit with one or more slave filters (27.1 – 27.n). The master control unit (36) comprises an integrator (30) having circuit elements (33, C) which match those elements of the slave filter (27.1 – 27.n) that define the slave filter's time constant (τ). Furthermore, the master control unit (36) comripses a voltage comparator (35) connected to an output (34) of the integrator (30), the voltage comparator (35) providing an output frequency signal (f_{com}), and a phase frequency comparator (PFC; 28) providing a control signal (υ) as output signal, the phase frequency comparator (PFC; 28) receiving said output frequency signal (f_{com}) and a reference frequency signal (f_{ref}) as input signals. The slave unit comprises said at least one slave filter (27.1 – 27.n), the slave filter (27.1 – 27.n) having a control signal input (41) for receiving said control signal (υ) thus allowing to calibrate the slave filter's transfer function by influencing the slave filter's time constant (τ).

Fig. 3

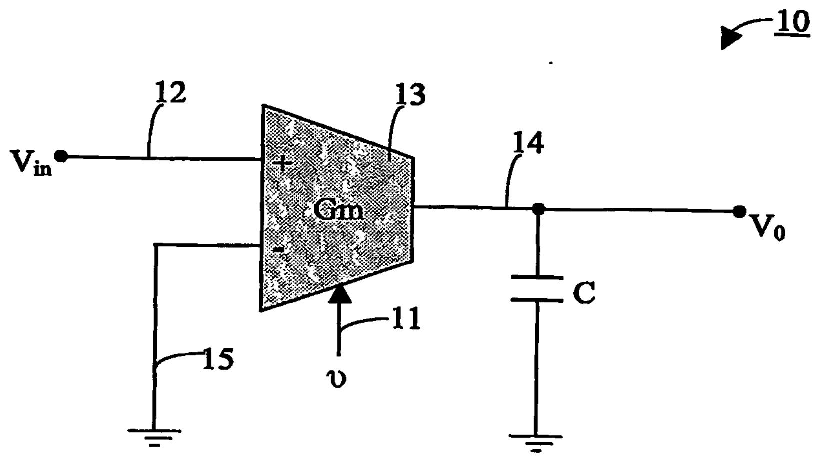


Fig. 1

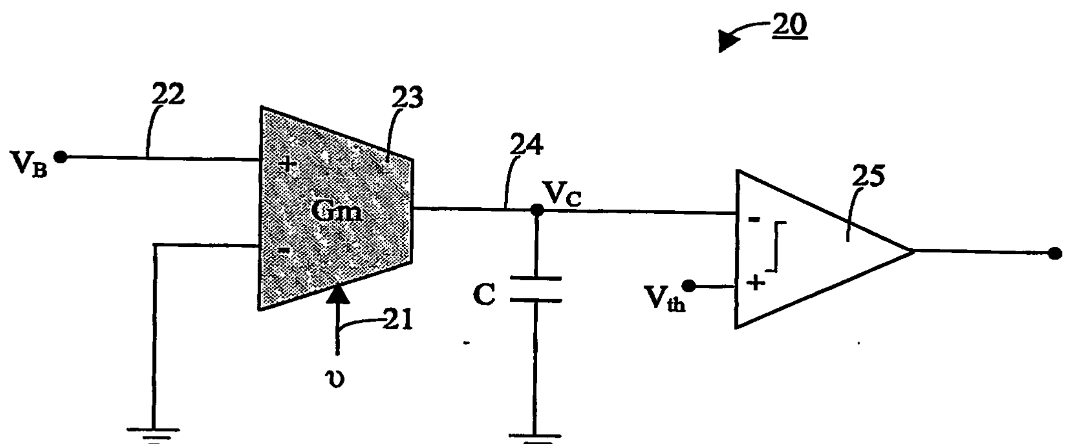


Fig. 2A

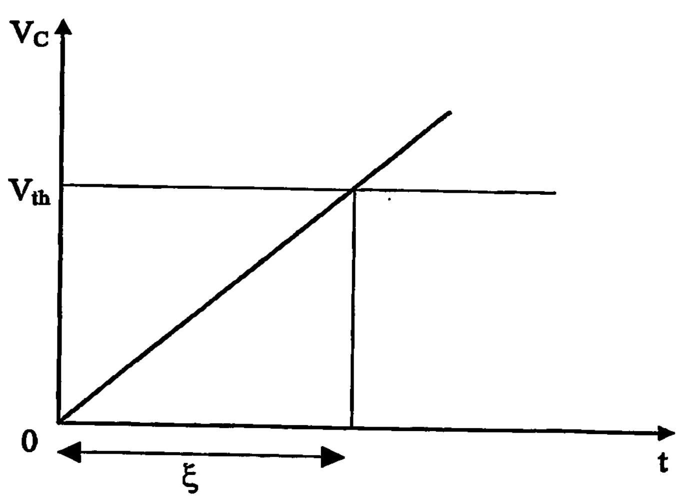
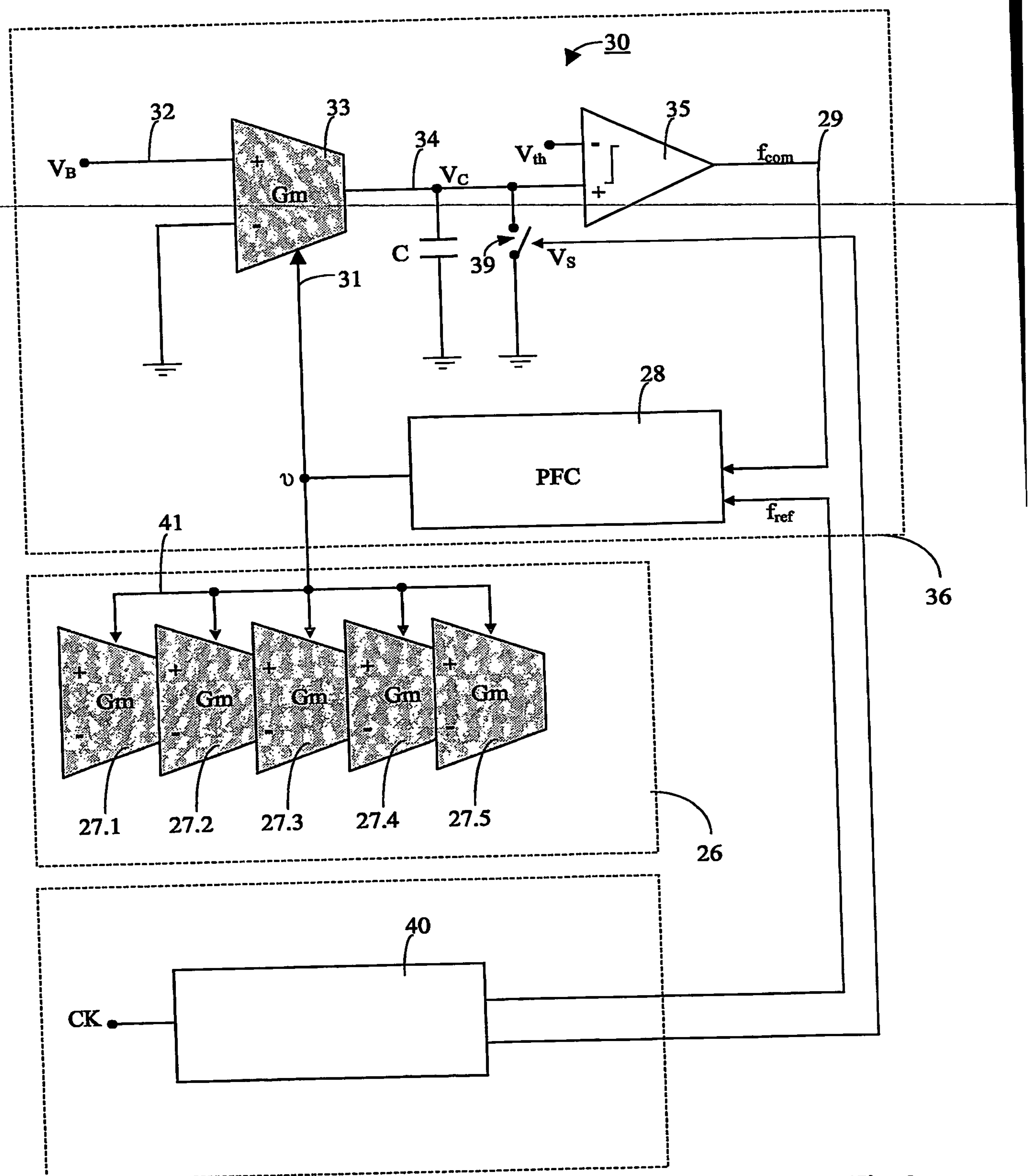


Fig. 2B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PFC
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27.2
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27.4
27.5
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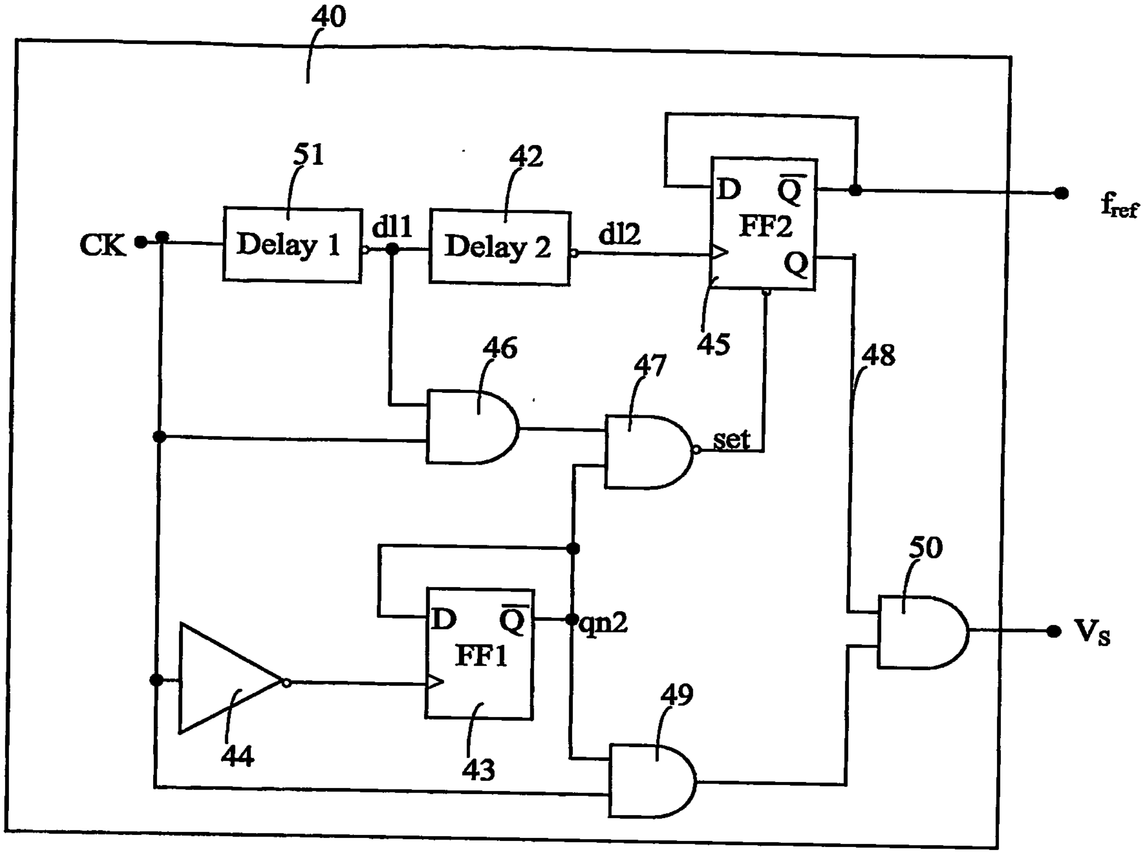
40
CK

Fig. 3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Delay 2
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dl1
dl2
D
Q̄
FF2
Q
fref
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47
set
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50
Vs
D
Q̄
FF1
qn2
44
43
49

Fig. 4A

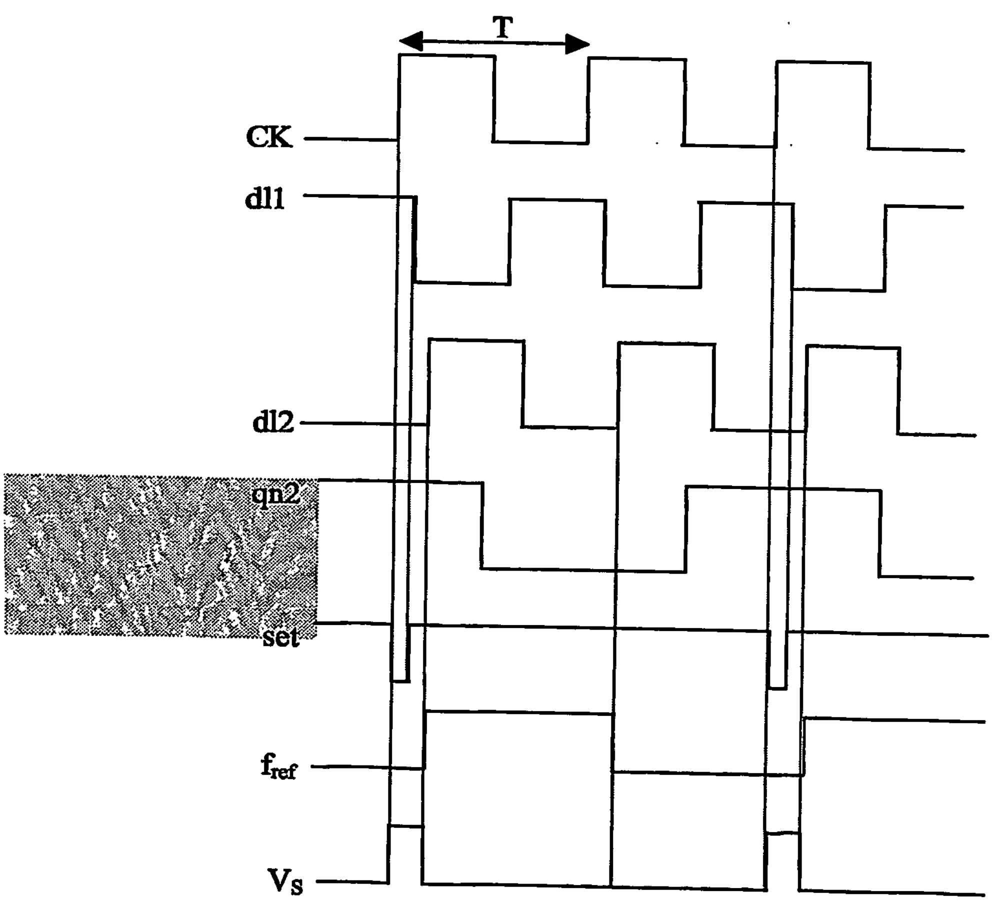
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Fig. 4B

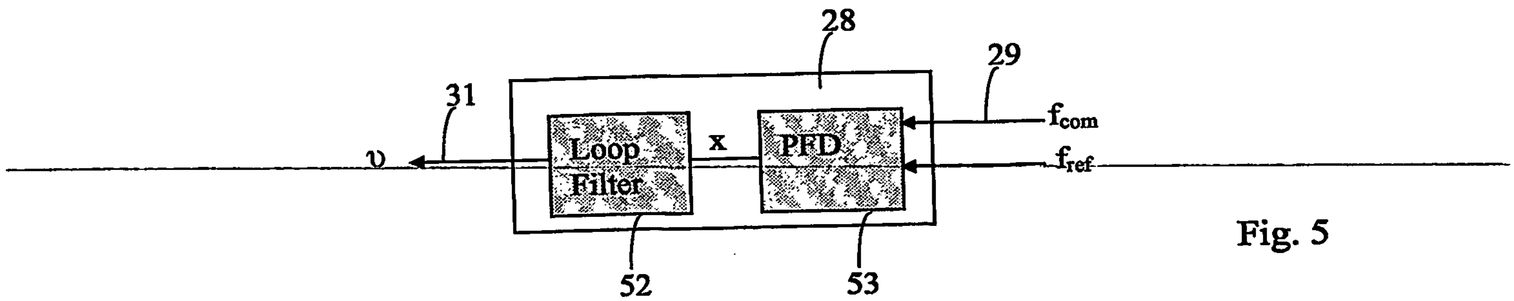
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Fig. 5

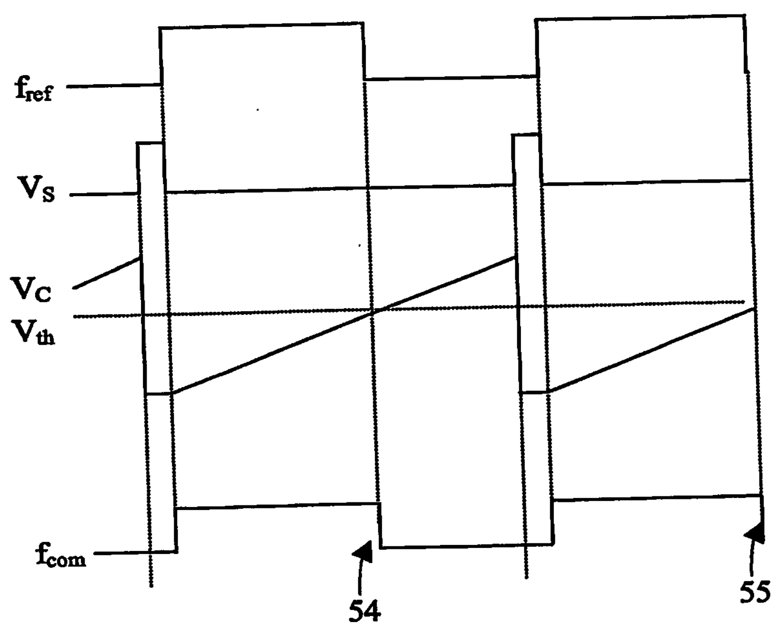
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Fig. 6

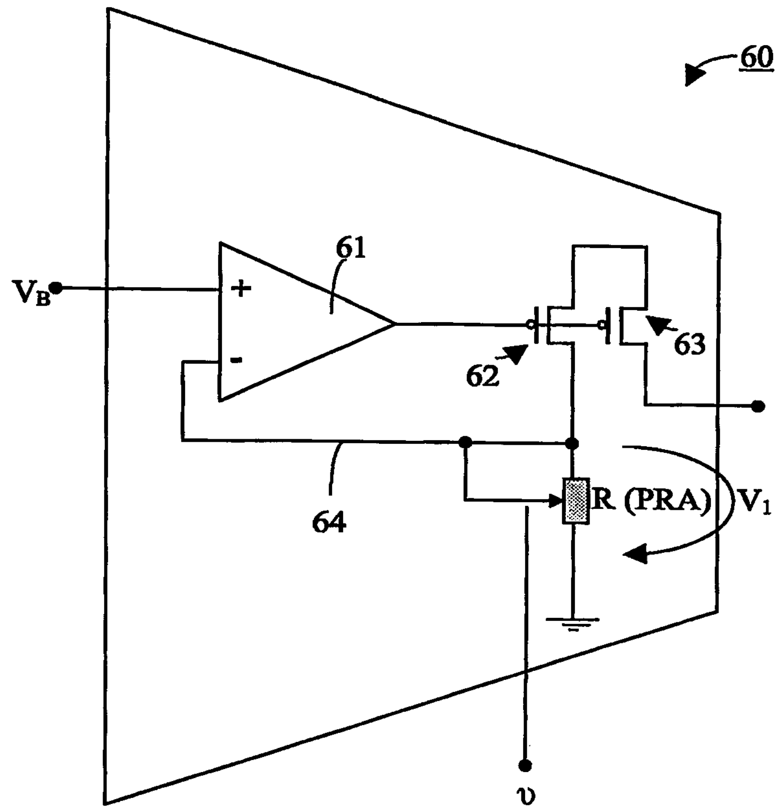

Fig. 7

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